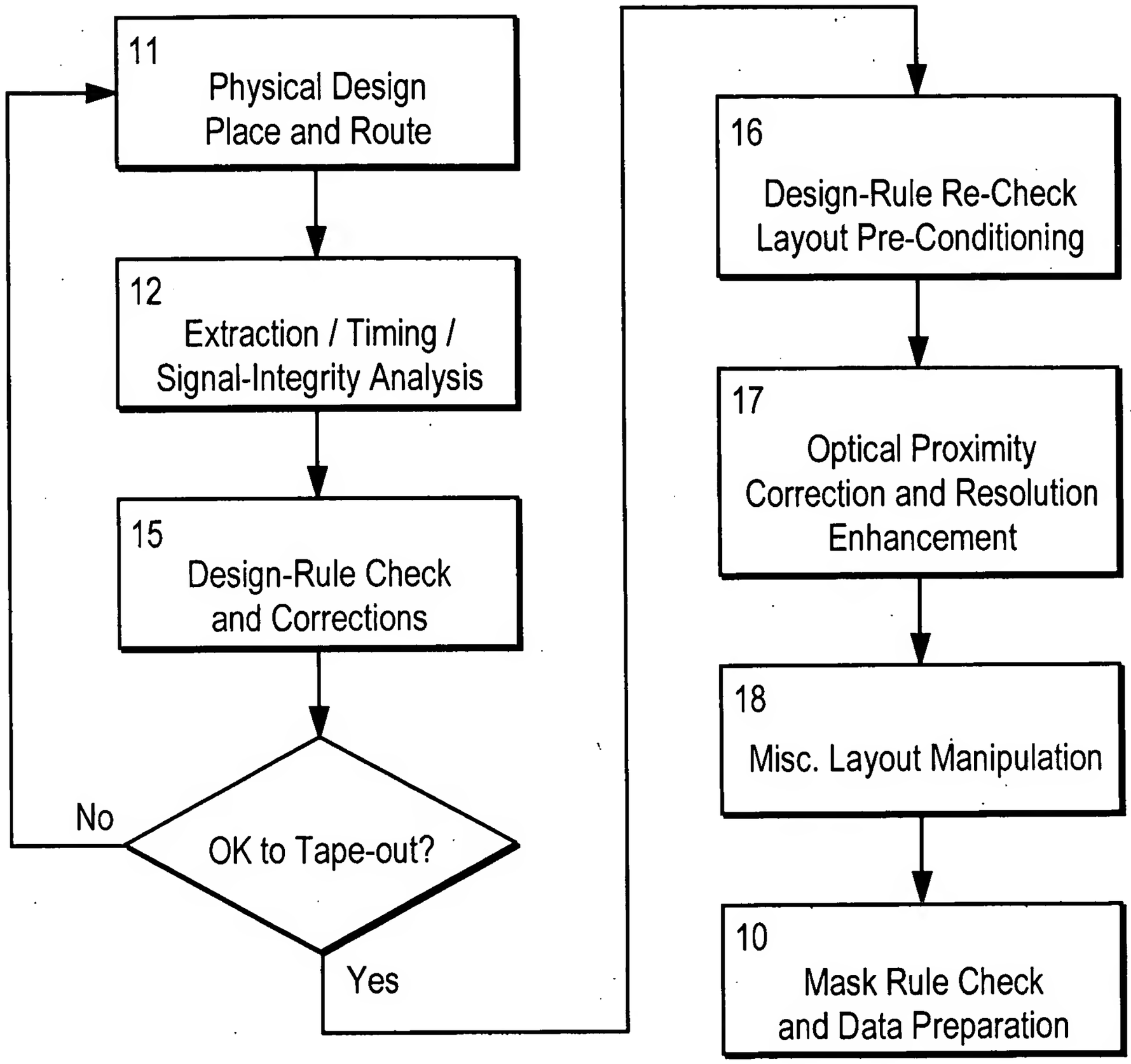

FIGURE 1
(PRIOR ART)

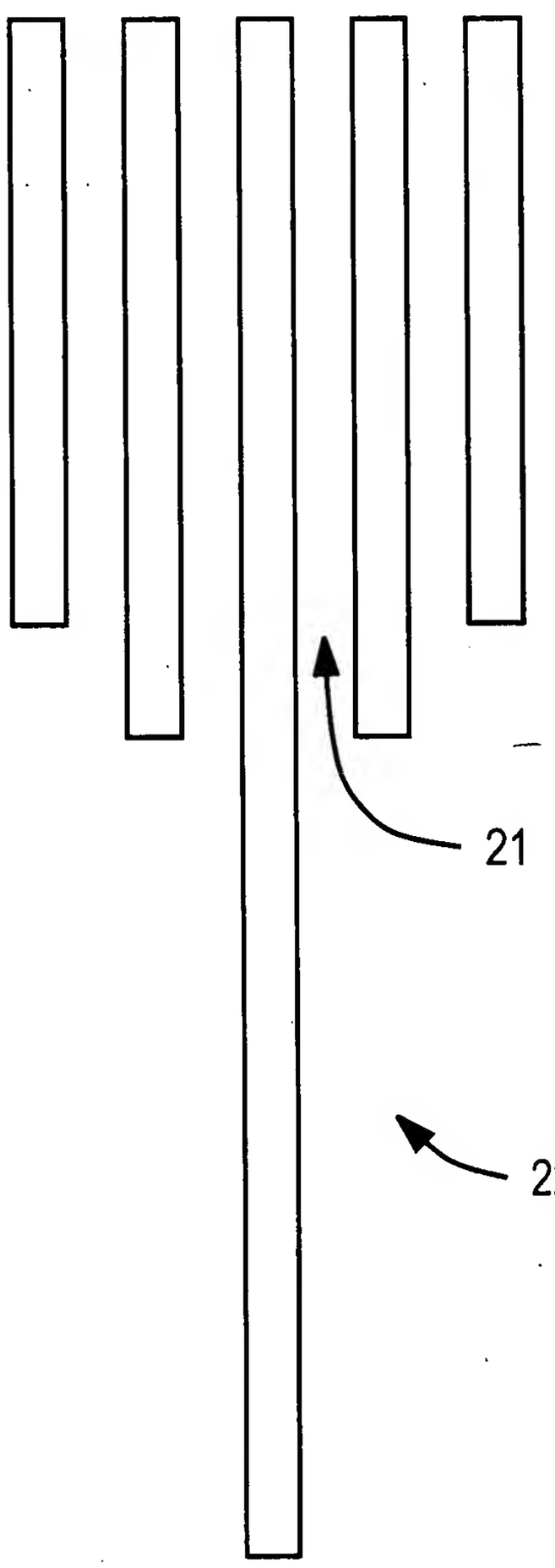

FIGURE 2A

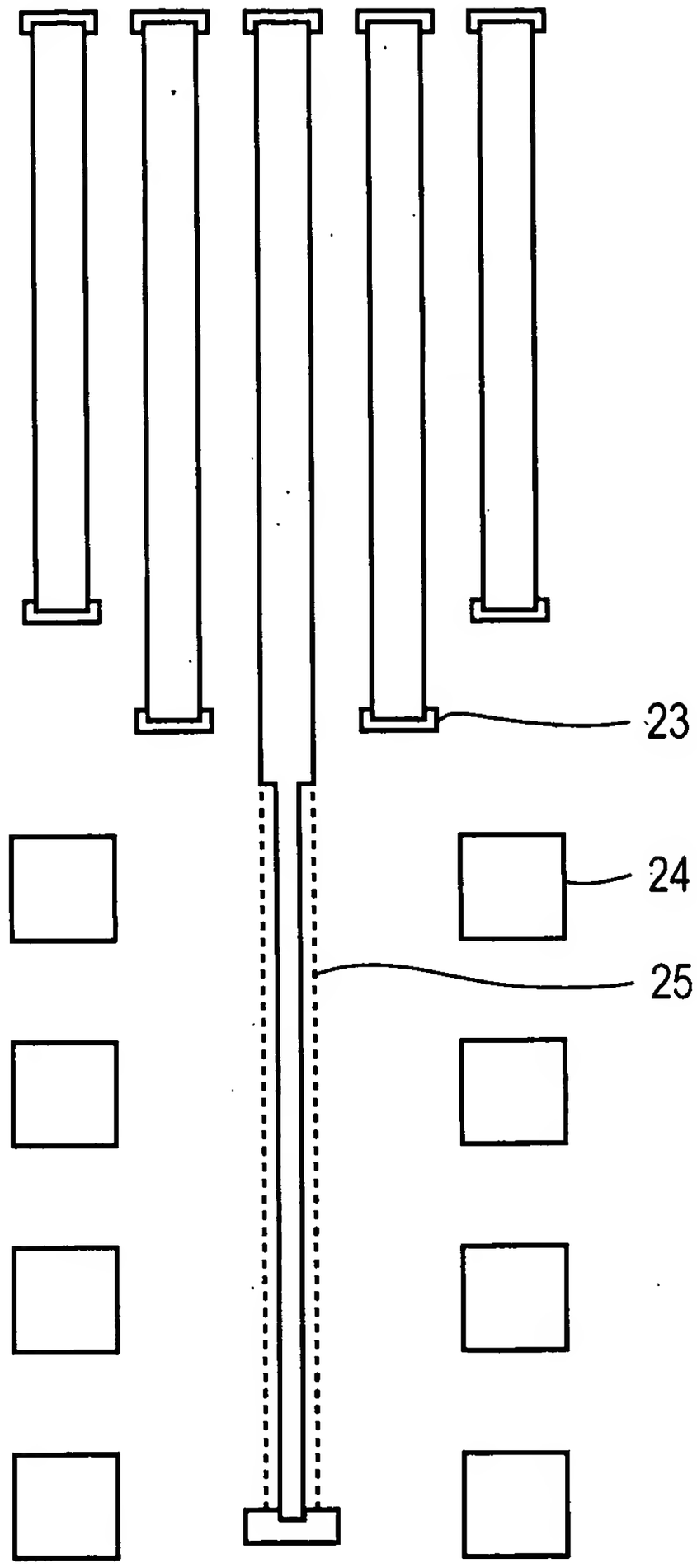

FIGURE 2B

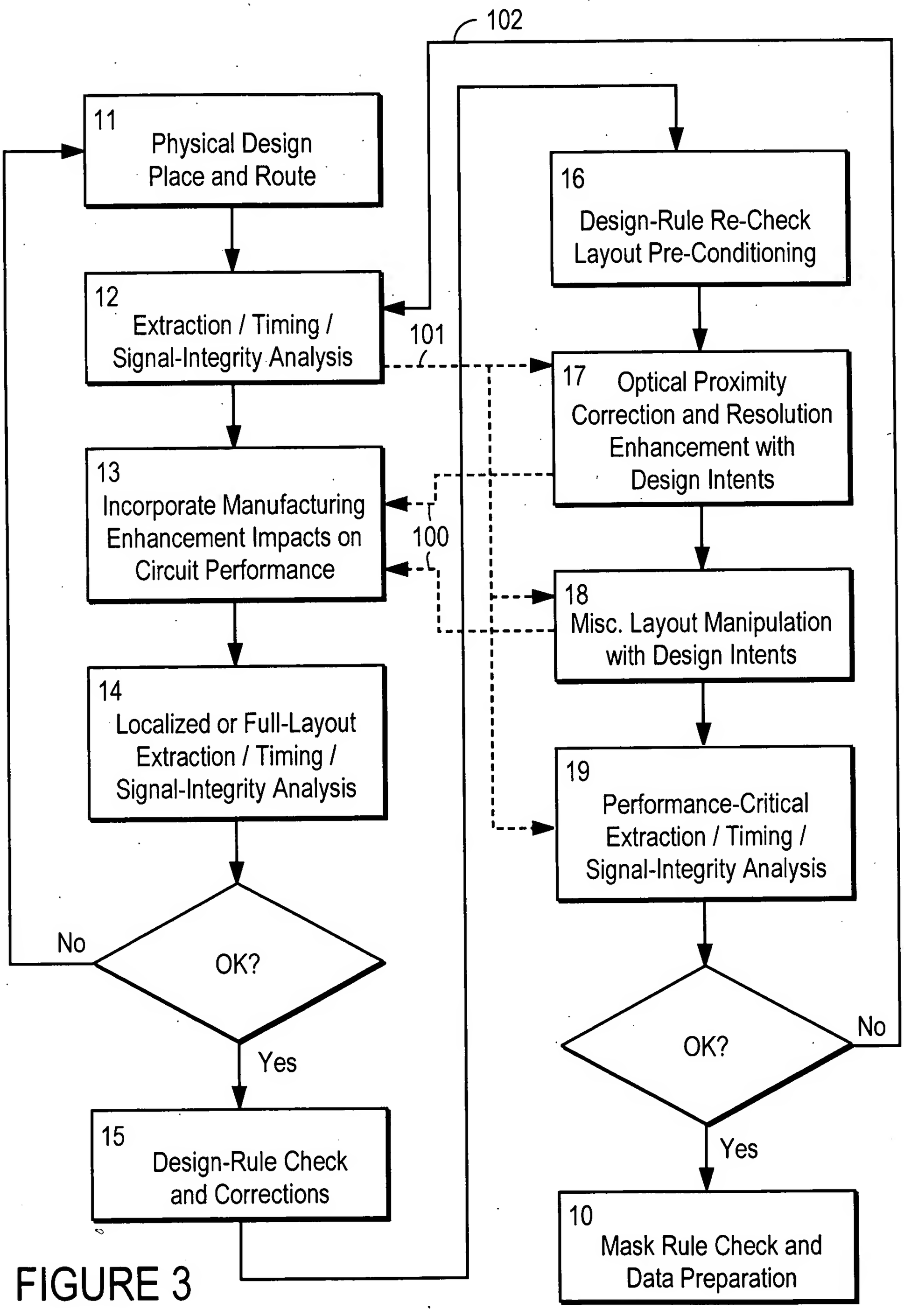
102
11
Physical Design
Place and Route
12
Extraction / Timing /
Signal-Integrity Analysis
101
13
Incorporate Manufacturing
Enhancement Impacts on
Circuit Performance
100
14
Localized or Full-Layout
Extraction / Timing /
Signal-Integrity Analysis
No
OK?
Yes
15
Design-Rule Check
and Corrections
16
Design-Rule Re-Check
Layout Pre-Conditioning
17
Optical Proximity
Correction and Resolution
Enhancement with
Design Intents
18
Misc. Layout Manipulation
with Design Intents
19
Performance-Critical
Extraction / Timing /
Signal-Integrity Analysis
OK?
No
Yes
10
Mask Rule Check and
Data Preparation

FIGURE 3

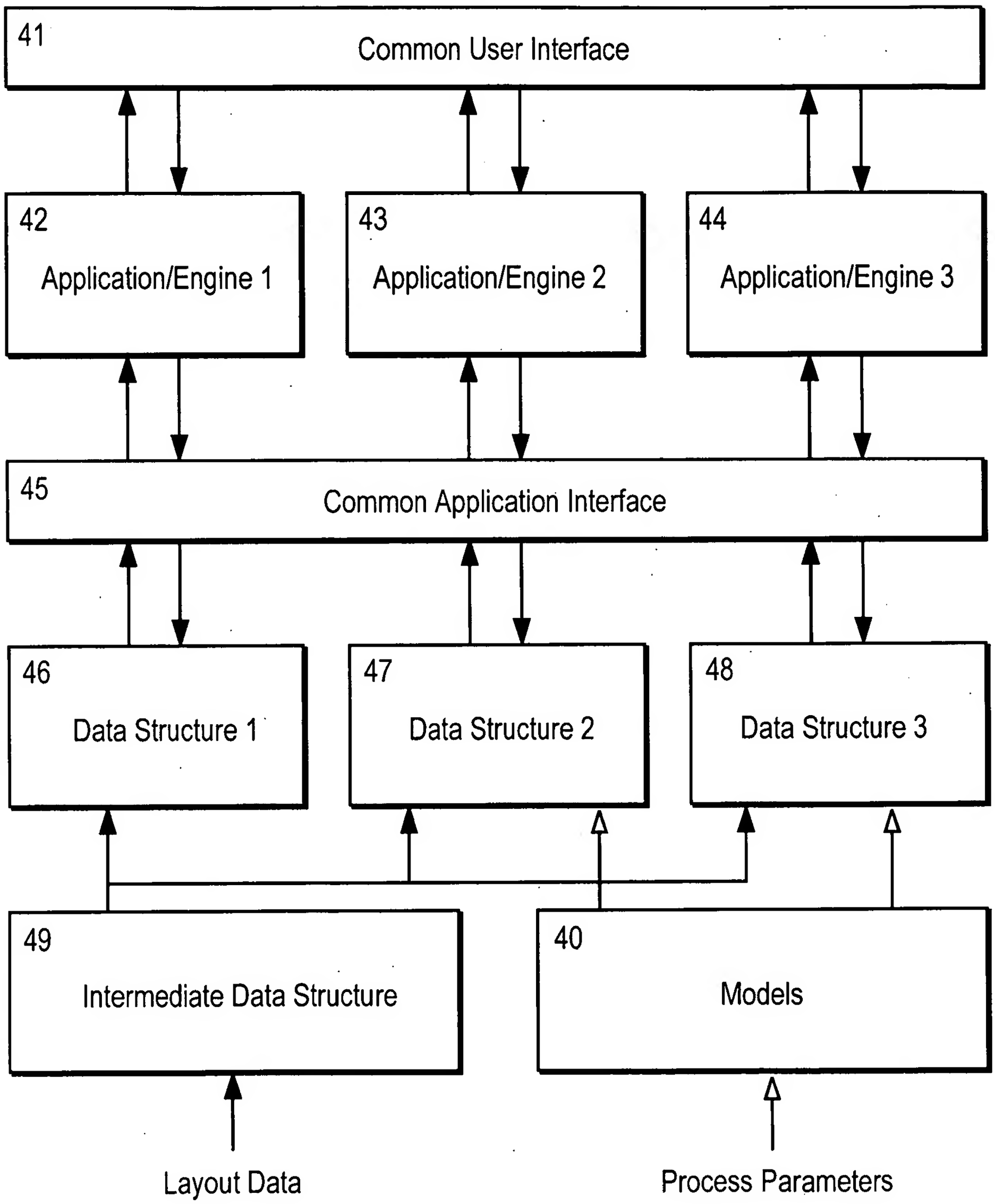
41
Common User Interface
42
Application/Engine 1
43
Application/Engine 2
44
Application/Engine 3
45
Common Application Interface
46
Data Structure 1
47
Data Structure 2
48
Data Structure 3
49
Intermediate Data Structure
40
Models
Layout Data
Process Parameters

FIGURE 4

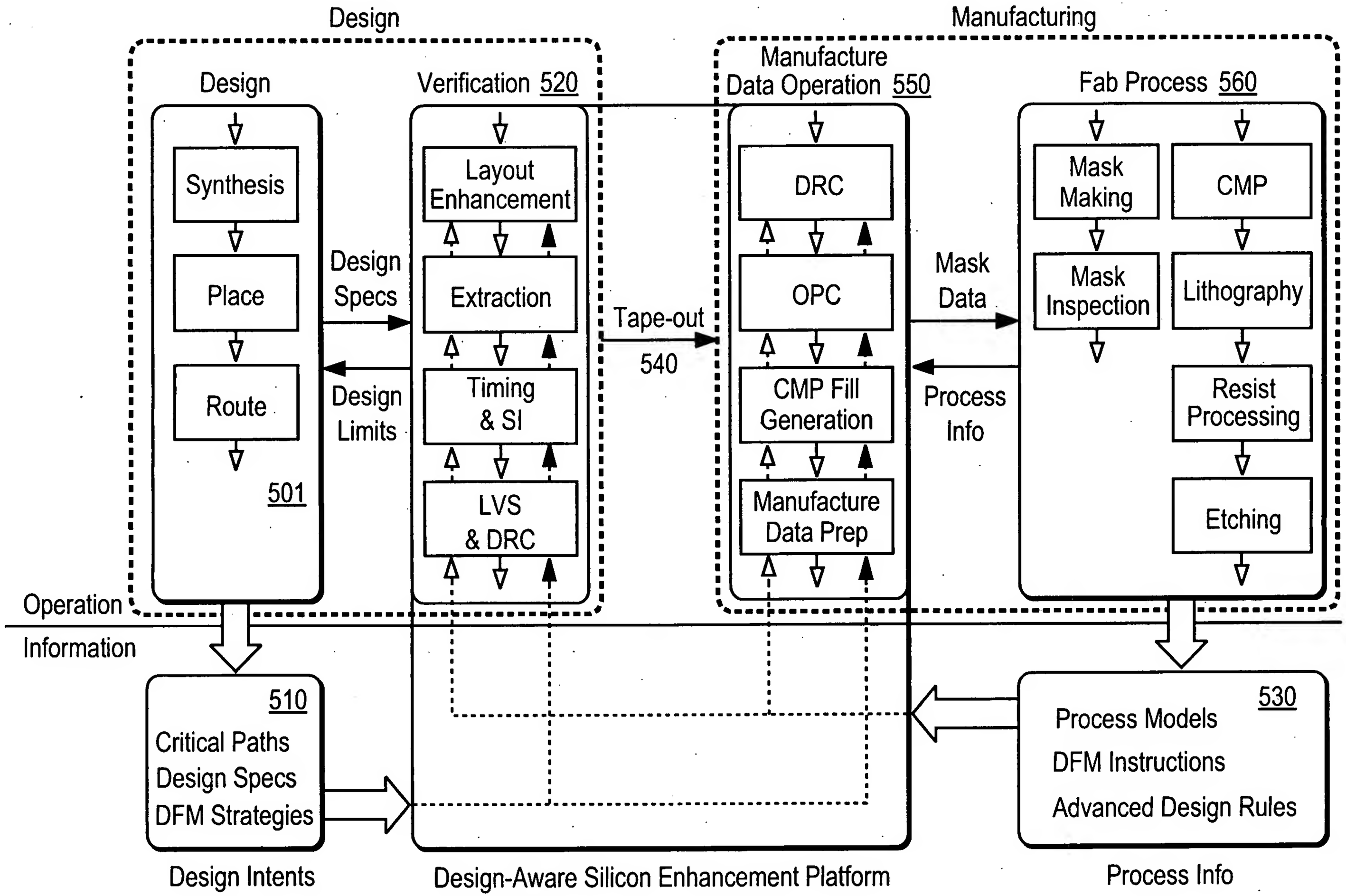

FIGURE 5

REPLACEMENT SHEET
Serial No.: 10/643,799
Title: Method and Platform for Integrated Physical Verifications and Manufacturing Enhancements
Inventor: Shao-Po Wu and Tsz-Tak Daniel Ho
Atty. Docket No.: 23875-09432
Sheet 5 of 5